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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,898	HOU, CHIEN-TZU	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☒ Claim(s) *1-3,5 and 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figure 8. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification including the claims is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

Abstract: lines 5-7 "the damage flip flops".

Specification: page 1 lines 7 and 8 "reduce the power as the IC is inoperative, and have an automatic repairing function as faults are found in a test."

page 1 line 12 " In concept of designing logic circuit"

page 2 lines 30-31 "This is why does a gated clock signal fclk can not be allowed in general logic circuits and is viewed it disobeys a design rule."

Other examples are given below in the list of claim objections.

Claim Objections

Claims 1-3, 5, and 9-11 are objected to because of the following informalities:

Claim 1 lines 5, 8, 9, 11, and 12 use the verb "being" which is not clear.

Claim 1 lines 1-2 state "while a system is boot up".

Claim 1 line 4 states "as faults occurs".

Claim 1 line 10 states "an buffer rearrange manager".

Claim 1 line recites the limitation " a buffer rearrange manager" it is unclear to the examiner if this is the same buffer rearrange manager in lines 10 and 11.

Claim 1 recites the limitation "assessing of data" however it is indicated that the data is being accessed and not assessed at this point.

Claim 2 line 2 states "the flip flops has a working frequency".

Claim 3 recites "a clock signal", it is unclear if this clock signal is the same as the gated clock signal of claim 2 or a separate clock signal.

Claim 5 line 2 states "the flip flops is a D type".

Claim 9 lines 2 and 3 state " a logic gate for integrating the output values of all flip flops" which is not clearly understandable.

Claim 10 line 5 states "forming a network type repairing" is unclear.

Claim 11 lines 5 and 10, use the verb "being" which is not clear.

Claim 11 line 1 " "a method for operation a self test and repairing data buffer".

Claim 11 line 5 states " all bit being '1' which are input each flip flop".

Claim 11 line 6 states "it representing at least one".

Claim 11 line 11 recites " all the flip flop can".

Claim 10 is objected to because of the following informalities: A claim cannot depend on itself. For purpose of examination it will be assumed applicant intended claim 10 to depend from claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the control" in line 2. There is insufficient antecedent basis for this limitation in the claim.

In claim 1 line 4 "*it* is repaired" There is no indication in the claim as to what "it" is being repaired. Also in line 12, "*it* being used" is unclear what is being used or if this is the same "*it*" referred to in line 4.

Claim 1 recites the limitation "the test result" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the repairing data" in 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitation "the previous stage" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites "a clock signal" in line 3. It is unclear if this clock signal is the same as the gated clock signal of claim 2 or a separate clock signal.

Claim 3 lines 3-6 recite the following features "wherein the latched write enable signal is generated by latch a write enable signal which controls the data writing of the flip flops and the latch enable signal is generated from the negative edge of system clock signal", which are completely unclear to the examiner.

Claim 10, line 2 "the output of the logic gate is used", it is unclear to the examiner which logic gate is specified here.

Claim 11 line 6 the term "it" is used and there is no indication in the claim as to what "it" is representing.

Claim 11 line 7 recites the limitation "the repairing unit". There is insufficient antecedent basis for this limitation in the claim.

Claim 11 lines 7 and 8 recite the limitation "replacing the flip flop", there is no indication as to what flip flop is being replaced.

Claims 2-10 are dependent on the independent claim 1 and inherit the 35 U.S.C. 112, second paragraph issues of the independent claim. As such, due to the ambiguities addressed above, the dependent claims will not be further considered with respect to prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Phan et al. U.S. Patent No. 6,505,313.

Phan et al teaches a memory device configured to detect changes in fault patterns. The memory device includes a memory array, a built-in selftest (BIST) unit, and a built-in self-repair (BISR) unit. The BIST unit runs test patterns on the memory array to identify faulty locations in the array. A comparator within the BIST or external to the BIST compares the actual output of the memory array to the expected output, and asserts an error signal whenever a mismatch occurs. The BISR unit intercepts addresses directed to the memory array, and operates on the addresses in three distinct phases. During a training phase, the BISR unit stores the intercepted addresses when the error signal is asserted. During the normal operation phase, the BISR unit compares all intercepted addresses to stored addresses and redirects a corresponding memory access if any intercepted address matches a stored address.

During a verification phase, the BISR unit compares intercepted addresses designated by assertions of the error signal to the addresses previously stored in the training phase. If the faulty intercepted address fails to match a stored address, the BISR unit asserts a "new error" signal. If at the end of the verification phase, a stored address has not matched any intercepted faulty address, the BISR asserts a "missed error" signal. In a modular element of a BISR circuit memory module, the element is configured to store faulty address locations and compare the stored faulty addresses with newly detected faulty addresses. This includes a multiplexer, an address latch, a reserve latch, and a compare gate. The multiplexer receives an output signal from the reserve latch, an input signal (IN), and an input select signal (ISEL). The output of the multiplexer is provided as an input (D) to the address latch. The address latch also receives a shift input signal (TI), a shift enable signal (TE), a clock signal (CLK), and a reset signal (RESET). When the shift enable signal (TE) and the reset signal (RESET) are de-asserted, a clock pulse causes the address latch to store the value of the input signal (D) and provide it as output signal (OUT). When the shift enable signal (TE) is asserted and the reset signal is de-asserted, a clock pulse causes the address latch to store the value of the shift input signal (TI). Assertion of the reset signal causes the output signal to be reset low. (See column 2 lines 25-48 Figure 3, column 6 lines 10-39)

Claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Barnes U.S. Patent No. 6,611,929.

Barnes teaches a test circuit for memory having plural memory cells and address latches responsive to addressing circuitry for reading/writing to said memory cells in a normal mode, has first connecting circuitry for connecting the address latches to form a linear feedback shift register. The linear feedback shift register is responsive to a clock signal to provide a sequence of addresses for testing the memory in a test mode. In the normal operational mode, the first inputs are set to the relevant address supplied by the address control and decoder circuitry and upon the next clock transition, the latches provide at their outputs the corresponding address. When it is desired to provide the built-in self test (BIST) function the control input which provides the control to the multiplexer, sets the multiplexers to output either their second, third or respectively fourth inputs depending upon whether the output sequence is desired in one sense, or the opposite sense. While the multiplexers pass their third inputs as their outputs, the address outputs of the latches sequence in a first direction to cover all of the memory addresses save the "0000" address, this being supplied by the fourth input. When the multiplexer pass their second inputs as their outputs, the address outputs sequence through in the reverse sense. There are also instances when all outputs are '0' and all outputs are '1'. (Column 1 lines 32-59, column 4 lines 3-17, Claims 5 and 7)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Permanent Error Log in an Adapter Card IBM Technical Disclosure Bulletin, NN9410657 October 1994, US VOL 37 ISSUE 10 PAGE 657 - 658

This paper describes a permanent error logging facility on a Micro Channel* adapter card for an IBM PS/2* computing system. This facility includes a first section for internal adapter errors detected by the microcode of the adapter card, and a second section for external errors also detected by the microcode of the adapter card. Internal errors are determined by this microcode to result from an internal adapter problem, while external errors are caused by an external problem, beyond the control of the adapter. Thus, when an error is detected by the adapter microcode during either POST (Power-On Self-Test), or during subsequent running in an operational mode, an error code is stored in this log, which is implemented within an EEPROM (Electrically Erasable Programmable Read Only Memory).

U.S. Patent No. 6,651,202 Phan

This patent teaches an integrated circuit includes built-in self test (BIST) and built-in self repair (BISR) circuitry, a fuse array capable of storing information related to defective memory locations identified during the manufacturing process. During manufacture, the integrity of the embedded memory of the integrated circuit is tested under a variety of operating conditions via the BIST/BISR circuitry. The repair solutions derived from these tests are stored and compiled in automated test equipment. If the repair solutions indicate that the embedded memory is repairable, the on-chip fuse array of the integrated circuit is programmed with information indicative of all of the detected

defective memory locations. The built-in self repair circuitry of the integrated circuit is not executed upon power up. Instead, the repair information stored in the fuse array is provided to address remap circuitry within the BISR circuit. When an access to one of these memory locations is attempted during normal operation of the integrated circuit, the BISR circuitry remaps the memory operation to a redundant memory element.

U. S. Patent No. 6,560,740 Zuraski

This patent teaches an apparatus and method are presented for programmable built-in self-test (BIST) and built-in self-repair (BISR) of an embedded memory (i.e., a memory formed with random logic upon a semiconductor substrate). A semiconductor device may include a memory unit, a BIST logic unit coupled to the memory unit, and a master test unit coupled to the BIST logic unit and the memory unit. The memory unit stores data input signals in response to a first set of address and control signals, and provides the stored data input signals as data output signals in response to a second set of address and control signals. The master test unit provides the memory test pattern to the BIST logic unit and generates the first and second sets of address and control signals. The BIST logic unit stores the memory test pattern, produces the data input signals dependent upon the memory test pattern, provides the data input signals to the memory unit, receives the data output signals from the memory unit, and compares the data output signals to the data input signals to form BIST results. The BIST system may perform a hardwired BIST routine when an asserted RESET signal is received by the semiconductor device and/or a programmable BIST routine under

software control. The BIST logic unit may include a redundant memory structure, and may be configured to functionally replace a defective memory structure of the memory unit with one of the redundant memory structures dependent upon the BIST results.

U.S. Patent No. 5,426,380 Rogers

This patent teaches a high speed processing flip-flop contains a header circuit and a pulse flip-flop circuit. The header circuit is a clock pre-processing circuit that generates clock pulses for operation of the pulse flip-flop circuit, and the pulse flip-flop circuit is a single stage latch. The header circuit contains functional logic including the flip-flop functionality for the high speed processing flip-flop, and any additional processing functions, such as multiplexing. The header circuit also contains a pulse modulator that generates selected clock pulses, based on the functional logic, for the pulse flip-flop circuit. The pulse flip-flop circuit contains storage, a driver circuit, and, for each data input, an input buffer, and a pass gate. The pulse flip-flop circuit couples the data to the driver circuit and storage during an active clock pulse for the corresponding data. Consequently, data input to the pulse flip-flop is not delayed by logic processing.

U.S. Patent No. 6,691,264 Huang

This patent teaches a "Wrapper" system and method are presented for integrating built-in self-test (BIST) and built-in self-repair (BISR) functions in a semiconductor memory device. The wrapper reduces the usual dependency of BISR circuitry on the BIST design, so that modifications and enhancements to the BIST may

be made without requiring significant changes to the BISR. A generic BIST engine with an extended address range (spanning both the accessible and the redundant rows) is used to test the entirety of memory as a single array, preferably using a checkerboard bit pattern. The memory is tested in two stages, using the same BIST algorithm. In the first stage, faulty rows in each memory portion are identified and their addresses recorded. At the end of the first stage a repair process allocates good redundant rows to replace faulty accessible rows. During the second stage, repair of the accessible memory portion is verified, while defects among the redundant portion are ignored. Compared to existing methods, the new method is believed to greatly simplify the interface between the BIST and the BISR circuitry, reduce the overall size of test and repair circuitry, and provide improved test coverage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
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